Saturday, Oct. 30, 2021 | 2021 年 10 月 30 日

Time	Event		
10:00-12:00	**Zoom Test**		
	10:00-11:00	**Session 1,2,3**	**ZOOM ID: 830 1184 8210**
		Session 4, 5	**ZOOM ID: 831 6876 1564**
	11:00-12:00	**Session 6,7,8**	**ZOOM ID: 830 1184 8210**
		Session 9,10	**ZOOM ID: 831 6876 1564**
		Keynote, Tutorial, Invited Speakers	**ZOOM ID: 856 2471 0254**
14:00-16:15	**Tutorials**		**ZOOM ID: 830 1184 8210**
	14:00-14:30	***Error Suppression Techniques for Energy-efficient High-resolution SAR ADCs*** Jiaxin Liu, University of Electronic Science and Technology of China, China	
	14:30-15:00	***Photoacoustic Imaging System towards More Miniaturization and Intelligence*** Fei Gao, ShanghaiTech University, China	
	15:00-15:15	Break	
	15:15-15:45	***Design of Low-Power PLL and CDR Integrated Circuits for High Speed Wireless/Wireline Communication*** Zhao Zhang, Institute of Semiconductors, Chinese Academy of Sciences, China	
	15:45-16:15	***High Performance CMOS RF/Millimeter-wave Voltage-controlled Oscillators*** Haikun Jia, Tsinghua University, China	

Sunday, Oct. 31, 2021 | 2021 年 10 月 31 日

Time	Event		
9:00-14:40	**Opening Ceremony &Keynote Speeches**		**ZOOM ID: 830 1184 8210**
	9:00-9:05	***Opening Remarks*** Xinglai Ge, Southwest Jiaotong University, China	
	9:05-9:45	***Keynote 1:Biosensors to Study, Treat and Predict Brain Disorders*** Mohamad SAWAN, Westlake University, China	
	9:45-10:25	***Keynote 2: Machine Learning for Microfluidic Design and Automation*** Tsung-Yi Ho, The Chinese University of Hong Kong	
	10:25-10:40	Break	
	10:40-11:20	***Keynote 3: AI Techology Applied in EDA Verfication*** Zhenghua Qi, Vice President of X-EPIC Corporation Limited, China	
	11:20-12:00	***Keynote 4: Circuit and Architecture of Intelligent Microprocessor*** Zhiyi Yu, Sun Yat-sen University, China	
	12:00-14:00	Break	
	14:00-14:40	***Keynote 5: Optimized Systolic Array Architecture for Compact CNNs*** Sheng Ma, National University of Defense Technology, China	
	14:40-15:00	Break	
15:00-17:30	**Invited Speech Session I:** ***Artificial Intelligent Technical for Circuit and System Design Automatic***		**ZOOM ID: 830 1184 8210**
	15:00-15:20	***In-Memory Computing towards the POS/w era——a Cross Layer Co-design Approach*** Li Jiang, Shanghai Jiao Tong University, China	
	15:20-15:40	***Novel Ways for Congestion Estimation and Routability Prediction*** Zhixiong Di, Southwest Jiaotong University, China	
	15:40-16:00	***The Three Waves of Applying Machine Learning in Routing Congestion Prediction*** Zhongdong Qi, Xidian University, China	
	16:00-16:10	Break	

16:10-16:30	***DNN Model Compression for IoT Domain Specific Hardware Accelerators*** Maurizio Palesi, University of Catania, Italy
16:30-16:50	***Solving Task Scheduling Problems for Mobile Edge Computing by Using Swarm Intelligent Algorithms*** Jin Sun, Nanjing University of Science and Technology, China
16:50-17:10	***Schedulability Analysis for Timed Automata with Tasks*** Jinghao Sun, Dalian University of Technology, China
17:10-17:30	***A Physics-Informed Recurrent Neural Network for RRAM Modeling*** Quan Chen, Southern University of Science and Technology, China

Monday, Nov. 1, 2021| 2021 年 11 月 1 日

Time	Event		
9:30-12:00	**Invited Speech Session II*: Advance Circuit and System Technology***		**ZOOM ID: 830 1184 8210**
	9:30-9:50	***Design and Evaluation of Fluctuating Power Logic to Mitigate Power Analysis at the Cell Level*** Fan Zhang, Zhejiang University, China	
	9:50-10:10	***Explorations on Content Addressable Memory Using Ferroelectric*** Xunzhao Yin, Zhejiang University, China	
	10:10-10:30	***Agile Generation of Mixed-Grained Reconfigurable Arrays*** Guojie Luo, Peking University, China	
	10:30-10:40	Break	
	10:40-11:00	***Approximate Arithmetic Circuits: A Review, Characterization and Recent Applications*** Jie Han, University of Alberta, Canada	
	11:00-11:20	***Algorithm-Circuit-Architecture Codesign Methodology for Energy Efficient Edge Deep Learning Accelerators*** Chixiao Chen, Fudan University, China	
	11:20-11:40	***Consideration of CDM Measurement for Bare Dies and Wafers*** Teruo Suzuki, Socionext Inc., Japan	
	11:40-12:00	***Cognitive SSD: from System to Chip*** Ying Wang, Institute of Computing Technology, CAS, China	
	12:00-13:30	Break	
13:30-18:10	**Oral Presentation Sessions**		
	13:30-15:45	**Session 1** *Embedded System and Intelligent Control*	**Session 2** *Microelectronics and Solid State Electronics*
		ZOOM ID: 830 1184 8210	**ZOOM ID: 831 6876 1564**
	15:45-15:55	Break	
	15:55-18:10	**Session 3** *Electronic Devices and Network Systems*	**Session 4** *Electronics and Electrical Engineering*
		ZOOM ID: 830 1184 8210	**ZOOM ID: 831 6876 1564**

Tuesday, Nov. 2, 2021| 2021 年 11 月 2 日

Time	Event		
9:30-17:55	**Oral Presentation Sessions**		
	9:30-11:45	**Session 5** *Computer and Electronic Engineering*	**Session 6** *Modern Information Technology and Application*
		ZOOM ID: 830 1184 8210	**ZOOM ID: 831 6876 1564**
	11:45-13:30	Break	
	13:30-15:30	**Session 7** *Circuit and System*	**Session 8** *Electronic Components Design and Testing*
		ZOOM ID: 830 1184 8210	**ZOOM ID: 831 6876 1564**
	15:30-15:40	Break	
	15:40-17:55	**Session 9** *Electronics and Power System*	**Session 10** *Computer and Information Engineering*
		ZOOM ID: 830 1184 8210	**ZOOM ID: 831 6876 1564**
18:10-18:30	**Closing & Awarding** ◆ Best Paper Award ◆ Best Presentation Award ◆ Outstanding Leadership Award		**ZOOM ID: 830 1184 8210**

Tutorial I

Error Suppression Techniques for Energy-efficient High-resolution SAR ADCs

Tutor: Jiaxin Liu, University of Electronic Science and Technology of China, China

14:00-14:30, Oct. 30, 2021

ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)

Abstract: The successive approximation register (SAR) is one of the most energy-efficient analog-to-digital converter (ADC) architecture for medium-resolution applications. However, its high energy efficiency quickly diminishes when the target resolution increases. This is because the SAR ADCs suffer from several major error sources, including the sampling kT/C noise, the comparator noise, and the DAC mismatch. These errors are increasing hard to be addressed in high-resolution SAR ADCs. This seminar introduces the recent advances on error suppression techniques for SAR ADCs, including the sampling kT/C noise reduction, the noise-shaping (NS) SAR, and the mismatch error shaping (MES). These techniques aim to boost the resolution of SAR ADCs while maintaining their superior energy efficiency.

Tutorial II

Photoacoustic Imaging System towards More Miniaturization and Intelligence

Tutor: Fei Gao, ShanghaiTech University, China

14:30-15:00, Oct. 30, 2021

ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)

Abstract: Combining light and sound, photoacoustic imaging is developing very fast in recent years, enabling high-resolution functional/molecular label-free biomedical imaging at centimetre's depth. In this tutorial, some new advances about photoacoustic imaging system towards more miniaturization and intelligence will be introduced, including three aspects:

Circuits and systems: As an emerging medical imaging modality, the PAI system design and optimization is of most significance. Particularly, the low-cost, miniaturization and integration of PAI system is highly desired for the wide deployment in both large hospitals and small clinics. In this tutorial, we will present several interesting circuits and system designs to achieve a lower cost and highly integrated PAI system. Topics include low-power laser system miniaturization, few-channel data acquisition integration, flexible ultrasound transducer array design, etc.

Artificial intelligence: It is inevitable that a lower cost and integration of PAI system will lead to sacrificed signal and image quality, such as lower signal-to-noise ratio, and limited-view image artifacts. To address these challenges, we will present several novel algorithm designs to improve signal/image quality. More importantly, we explored several novel deep learning frameworks for PA image reconstruction, quantification, classification, segmentation, and PAI assisted light/sound treatment.

Biomedical applications: Last but not least, several most potential biomedical applications of PAI will be introduced. Compared with widely used medical imaging modalities, such as B-mode ultrasound, X-ray CT, MRI, the unique advantage of PAI is the rich optical contrast at deep tissue (>5 cm), which may enable higher diagnostic accuracy of critical diseases, such as cancer. In this tutorials, we will briefly introduce several application scenarios of PAI in early-stage breast cancer screening, ring-shape neck imaging, microscopic skin imaging, and endoscopic imaging probe for esophagus cancer detection.

Tutorial III

Design of Low-Power PLL and CDR Integrated Circuits for High Speed Wireless/Wireline Communication

Tutor: Zhao Zhang, Institute of Semiconductors, Chinese Academy of Sciences, China

15:15-15:45, Oct. 30, 2021

ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)

Abstract: To further increase the data-rate of the 5G wireless transceiver (e. g. > 10Gb/s), an ultra-low-jitter phase-locked loop (PLL) with sub-100-fs integrated jitter and low power consumption is required to generate a clean LO signal. This significantly challenges the PLL design. Meanwhile, the four-level pulse-amplitude modulation (PAM4) clock-and-data recovery circuit (CDR), which is the key sub-system of the PAM4 transceiver, is usually more power-hungry due to the more complicated circuit topology.

In this tutorial, we firstly give a brief review of the basics and design considerations of the low-jitter & low-PLL and PAM4 CDR. Then, several the low-power design techniques of the ultra-low-jitter PLL and PAM4 CDR are introduced based on our recent research results, including 2 PLLs and 3 PAM4 CDRs.

Tutorial IV

High Performance CMOS RF/Millimeter-wave voltage-controlled Oscillators

Tutor: Haikun Jia, Tsinghua University, China

15:45-16:15, Oct. 30, 2021

ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)

Abstract: RF/Millimeter-wave voltage-controlled oscillators (VCO) are one of the critical components in 5G communication. On one hand, a wide frqeuency tuning range is desired to cover varies allocated 5G frequency bands. On the other hand, a low phase noise performance is also desired to support the advanced signal modulation. This presentation will talk about the wide frequency range and low phase noise VCO design techniques in CMOS process. One presented VCO achieves a frequency tuning range from 8.2 GHz to 21.5 GHz, while the other one achieves a low-phase-noise performance of -104.72dBc/Hz at 1MHz offset from 59.12GHz carrier frequency.

Biosensors to Study, Treat and Predict Brain Disorders

Mohamad SAWAN, Fellow of IEEE
Westlake University, China
9:05-9:45, Oct. 31, 2021
ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)

Keynote I

Abstract: Neural cells originated brain diseases are becoming the focus of advanced multidisciplinary research topic to recover neurological orders. Seizures, addictions, stroke, blindness, etc, are refractory to surgical, and to advanced pharmaceutical solutions. Biosensors to collect data from various body regions (EEG, ECG, ENG, EcoG, EMG, etc) and from local neural cells (Ions, action potentials, single cell, field potential, neural multiunits, etc) and real-time analyze them could facilitate identifying the origin of these numerous brain diseases. These measurements are also used to detect biomarkers and use them for data classifications and subsequent use for decoding status, delivering instructions to augment learning process and improving neural functions. Also, evolution and prediction of diseases is becoming mandatory to improve healthcare processing. Many industrial and academic groups are building varieties of processors and system-on-chip based platforms that include machine and deep learning methods. However, the latest are either very large silicon areas and or require large power budget to operate. These features are not convenient for brain-level applications. This talk includes the description of a neurorecording system-on-chip platforms, neurotransmitters detection and manipulation, cultured neural cells training and analysis, Coronavirus early and accurate detection. Also, parts of research directions are intended to predict seizures, stroke and bladder dysfunctions evolutions. In addition, will report novel technique to speed up the detection of emerging COVID-19 and corresponding mutations.

Machine Learning for Microfluidic Design and Automation

Tsung-Yi Ho, The Chinese University of Hong Kong
9:45-10:25, Oct. 31, 2021
ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)

Keynote II

Abstract: Microfluidics or Lab on a Chip (LoC) system provides a powerful integrated platform for automated manipulation of different solutes, droplets, particles or even tissue at the microscale. Unlike conventional microfluidic devices, current LoC systems usually have multiple units with various functionalities, which requires microfluidic-oriented design automation tools to facilitate researchers during the design process. To address this issue, machine learning techniques might be a promising solution for microfluidics/LoC design automation with its ability to learn from both experimental data and numerical data. In this talk, different aspects related to this field will be presented and discussed.

AI Techology Applied in EDA Verfication

Keynote III

Zhenghua Qi, Vice President of X-EPIC Corporation Limited, China
10:40-11:20, Oct. 31, 2021
ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)

Abstract: As the complexity of SoC design is increasing significantly, the verification becomes more and more critical. Today, verification work spans almost all stages of the entire chip design flow. It therefore consumes the most time during the whole chip design cycle.

Each design stage requires specific verification methods and tools to solve different problems arising in that stage. All those methods and tools need to co-work in a manner to give the best overall performance. Therefore, verification methodology and corresponding EDA tool play an important role in the verification closure. This presentation first covers traditional verification concepts and ways to increase the verification efficiency. It also illustrates some unique challenges facing EDA verification tool and explores some possible solutions based on AI technology.

Circuit and Architecture of Intelligent Microprocessor

Keynote IV

Zhiyi Yu, Sun Yat-sen University, China
11:20-12:00, Oct. 31, 2021
ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)

Abstract: Processors are facing great challenges and opportunities. This talk will discuss the challenges, opportunities, and some design cases of intelligent microprocessors. 1) With the increasing number of cores/modules of microprocessors, efficient interconnect has become a key problem. We will discuss the on-chip and inter-chip interconnect techniques including the router design, the network flow control mechanism, and the design process and circuits for data-driven asynchronous interconnection. 2) The brain-like spiking neural networks provide another view for the future intelligent processors. We will discuss the design of neurons cores and system architecture of spiking networks, to show its potential advantages in energy efficiency.

Optimized Systolic Array Architecture for Compact CNNs

Sheng Ma, National University of Defense Technology, China
14:00-14:40, Oct. 31, 2021
ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)


Keynote V

Abstract: The systolic array architecture is one of the most popular choices for convolutional neural network hardware accelerators. The biggest advantage of the systolic array architecture is its simple and efficient design principle. Without complicated control and dataflow, hardware accelerators with the systolic array can calculate traditional convolution very efficiently. However, when computing compact CNNs, such as the small-scale convolution or depthwise convolution, the processing element (PE) utilization rate of the array decreases sharply. The main reason is that the simple architecture design limits the flexibility of the systolic array.

To address these issues, we propose two types of optimized systolic array architectures, including a configurable multi-directional systolic array (CMSA) and a heterogeneous systolic array architecture. Both optimizations can significantly improve the performance of the systolic array for processing compact CNNs. Meanwhile, the hardware overheads of both designs are minor.

Invited Speech Session I

Artificial Intelligent Technical for Circuit and System Design Automatic

Hosts: Xiaohang Wang, South China University of Technology

Jinyu Zhan, University of Electronic Science and Technology of China

15:00-17:30, Oct. 31, 2021

ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)

	15:00-15:20	***In-Memory Computing towards the POS/w era——a Cross Layer Co-design Approach*** Li Jiang, Shanghai Jiao Tong University, China
	15:20-15:40	***Novel Ways for Congestion Estimation and Routability Prediction*** Zhixiong Di, Southwest Jiaotong University, China
	15:40-16:00	***The Three Waves of Applying Machine Learning in Routing Congestion Prediction*** Zhongdong Qi, Xidian University, China
Break		
	16:10-16:30	***DNN Model Compression for IoT Domain Specific Hardware Accelerators*** Maurizio Palesi, University of Catania, Italy
	16:30-16:50	***Solving Task Scheduling Problems for Mobile Edge Computing by Using Swarm Intelligent Algorithms*** Jin Sun, Nanjing University of Science and Technology, China
	16:50-17:10	***Schedulability Analysis for Timed Automata with Tasks*** Jinghao Sun, Dalian University of Technology, China
	17:10-17:30	***A Physics-Informed Recurrent Neural Network for RRAM Modeling*** Quan Chen, Southern University of Science and Technology, China

Invited Speech Session II

Advance Circuit and System Technology

Host: Letian Huang, University of Electronic Science and Technology of China

9:30-12:00, Nov.1, 2021

ZOOM ID: 830 1184 8210 (https://us02web.zoom.us/j/83011848210)

	9:30-9:50	***Design and Evaluation of Fluctuating Power Logic to Mitigate Power Analysis at the Cell Level*** Fan Zhang, Zhejiang University, China
	9:50-10:10	***Explorations on Content Addressable Memory Using Ferroelectric*** Xunzhao Yin, Zhejiang University, China
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