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Lecture by

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Computing in memory for edge neural networks

Abstract: Utilizing emerging nonvolatile memories, particularly, with the computing-in-memory architecture, to accelerate deep neural networks (DNNs) has been considered as a promising approach to solve the bottleneck of “memory wall” in Von Neumann architecgure. Realization of the unity of computing and memory in the same place has opened up a promising research direction to reduce the data transfer and the related power consumption. According to the principle for MAC operations in DNN, the state-of-the-art techniques can be mainly divided into three routes. The first one is based on the “stateful logic” paradigm, which can realize Boolean logic within one or several memory cells. The second one is a reading-based method. By putting one of the operands into the sensing amplifier, it can also achieve Boolean logic with the content in the memory cell. These two methods are still in a “digital” way, and they realize MAC computing through row-by-row read/write operations. The last one is an “analog-like” method. By transforming the digital input signals into multi-level voltage signals, and applying them to the different rows of the memory array, the MAC results can be obtained in different columns with analog to digital converter (ADC). In this talk, we will review the main research status and challenges of DNN accelerators with computing in memory architecture.

Prof. Wang KANG received the joint double Ph.D degrees in physics from University of Paris-Sud, France, and in Microelectronics from Beihang University, China. He is now an Associate Professor in School of Microelectronics at Beihang University. He research interest includes spintronics and its related devices, circuits and architectures. He has co-authored 3 book chapters, 20 Chinese patents and over 80 scientific papers, including Nature Electronics, Proceeding of the IEEE, IEEE Trans. Circ. Syst. I: Reg. Papers, IEEE Trans. Computers, IEEE Trans. Electron Devices, IEEE Electron Devices Lett., Physical Review Applied, DAC, DATE, ASP-DAC, GLSVLSI etc. He has been severing as guest editors of “SPIN” and “Microelectronics Journal”. He is a Senior Member of IEEE.